

FIG.1

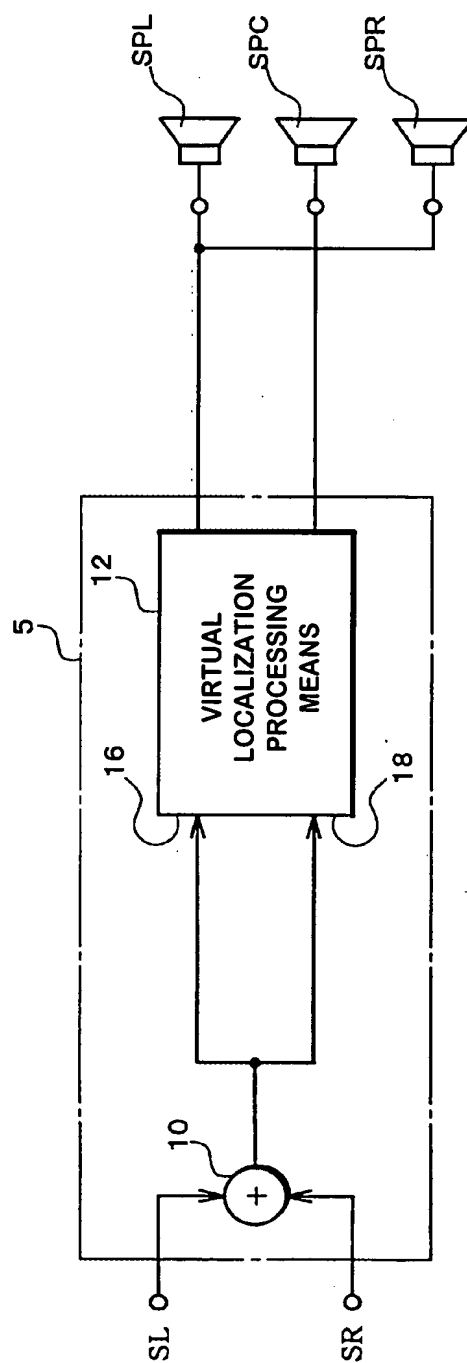


FIG.2

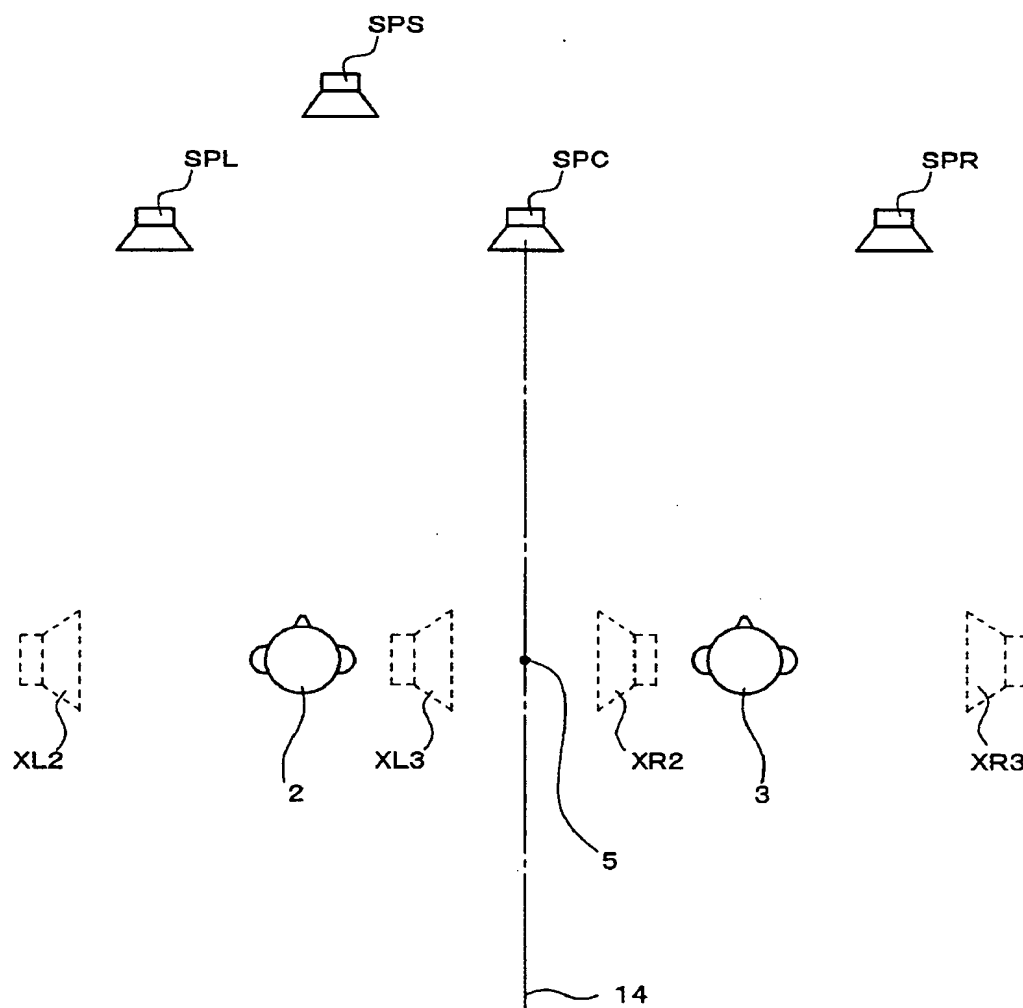


FIG.3A

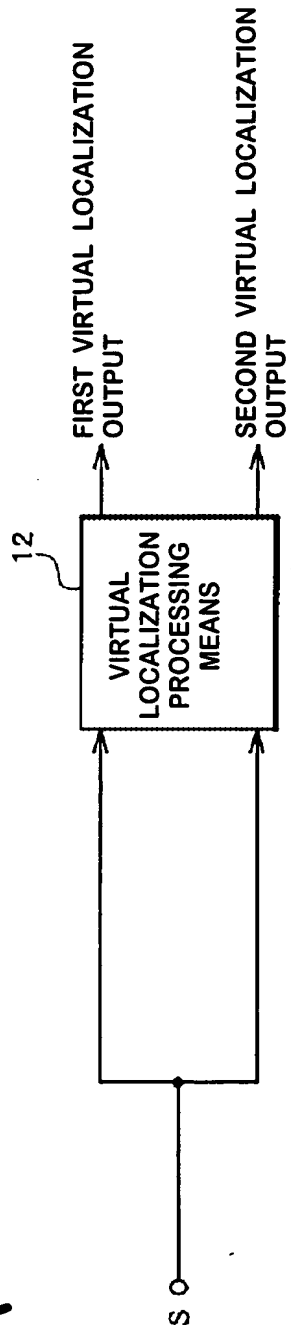


FIG.3B

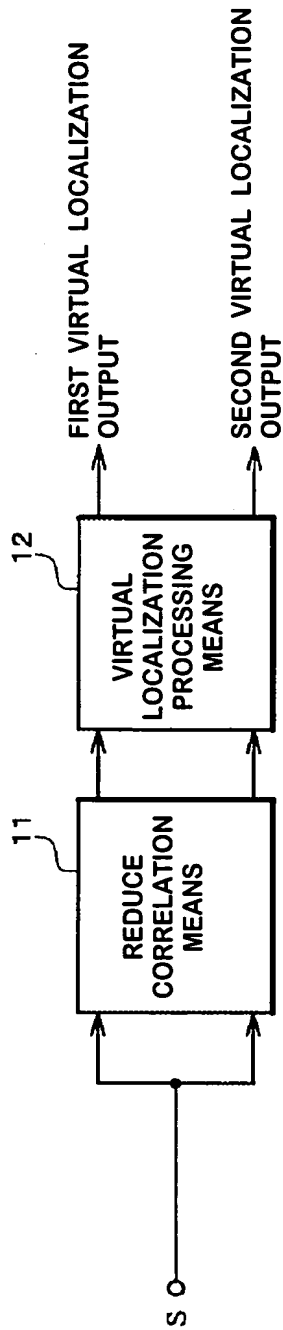


FIG.3C

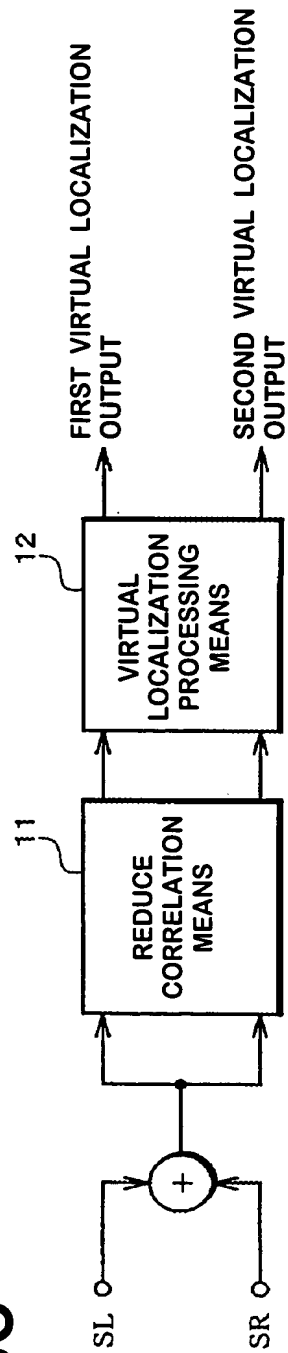


FIG.4

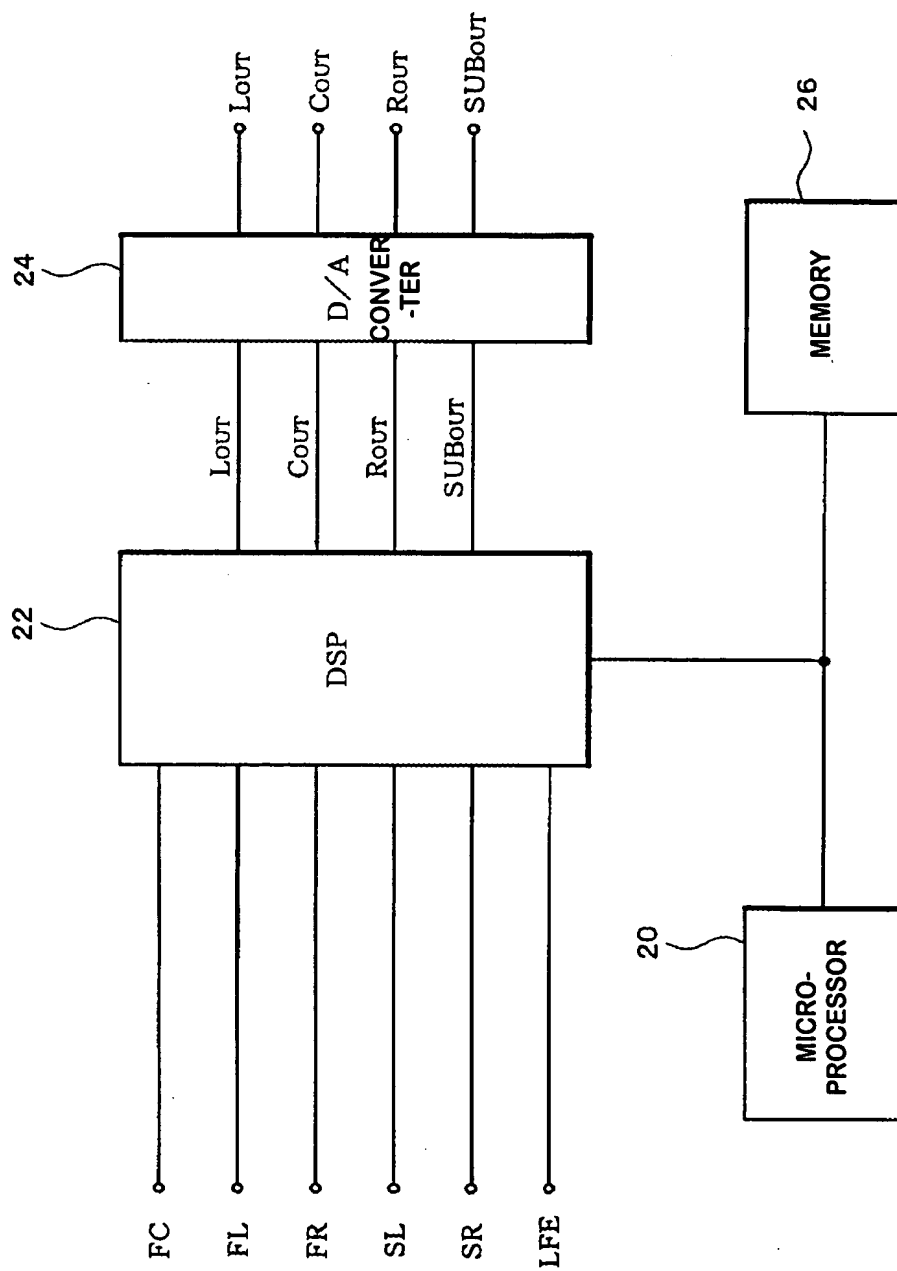


FIG.5

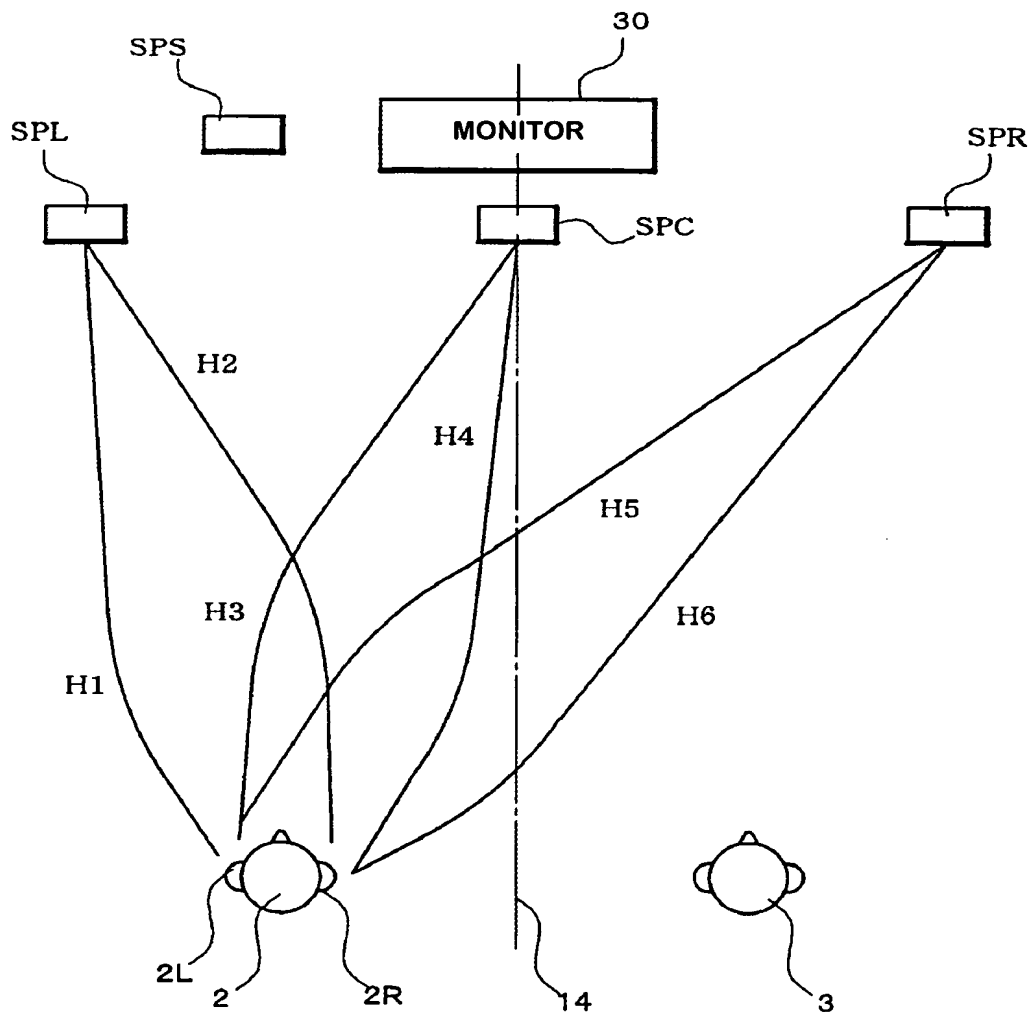


FIG.6

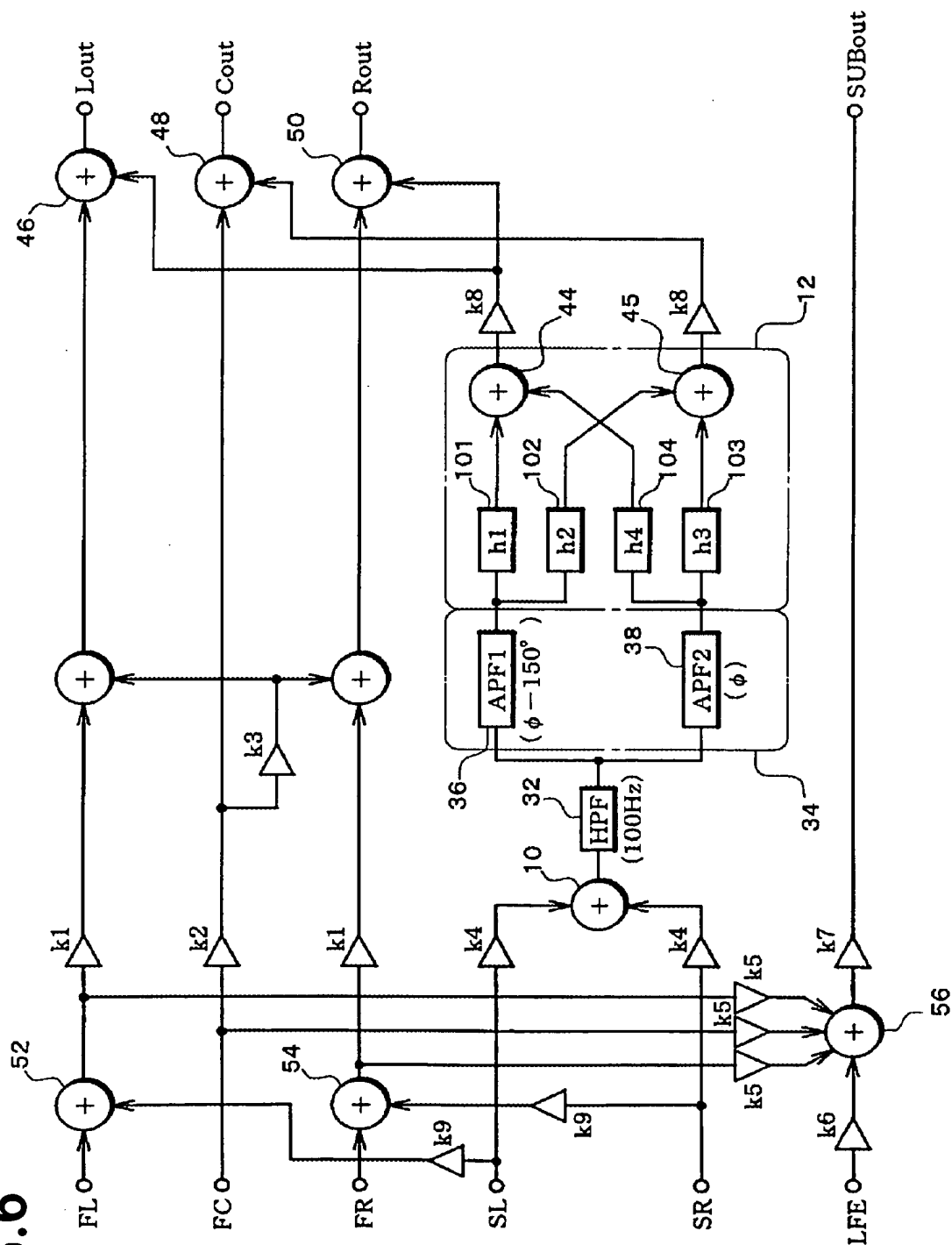


FIG.7A

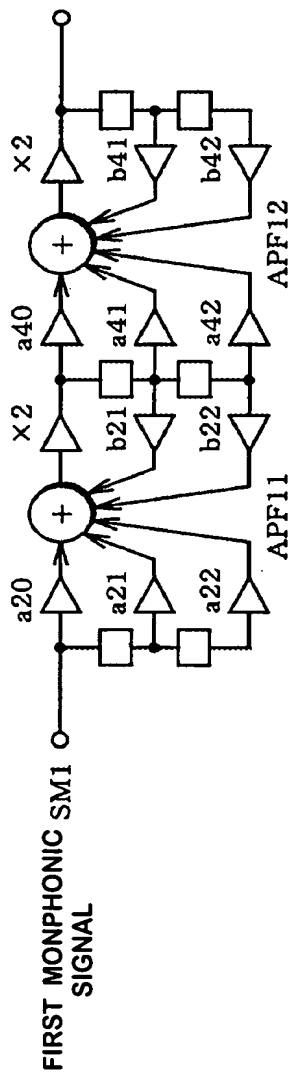


FIG.7B

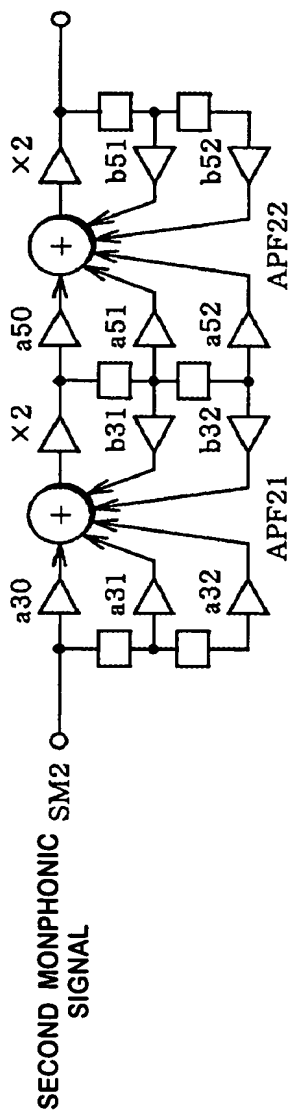


FIG.8

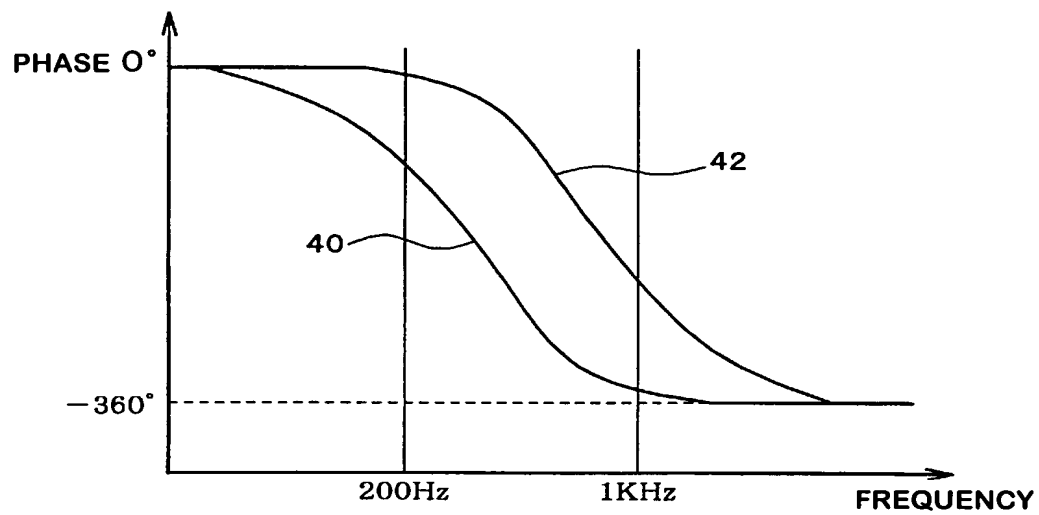




FIG.9

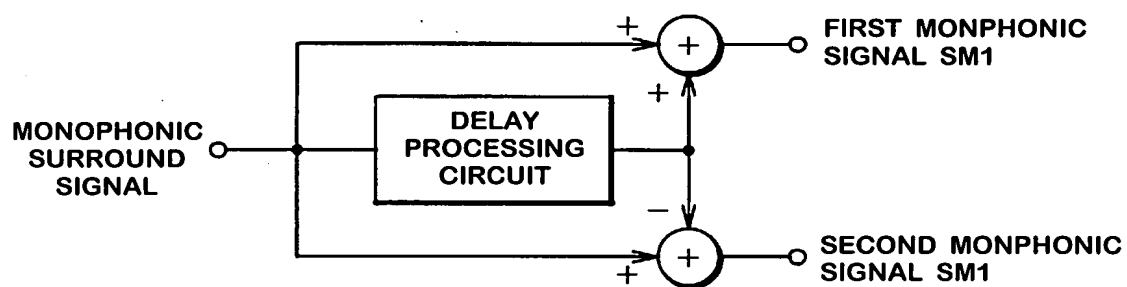


FIG.10

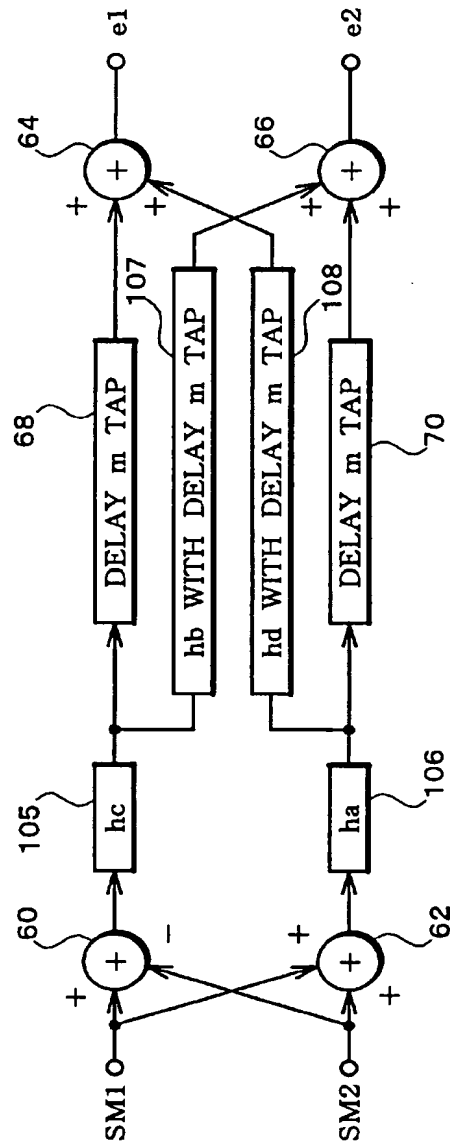


FIG.11

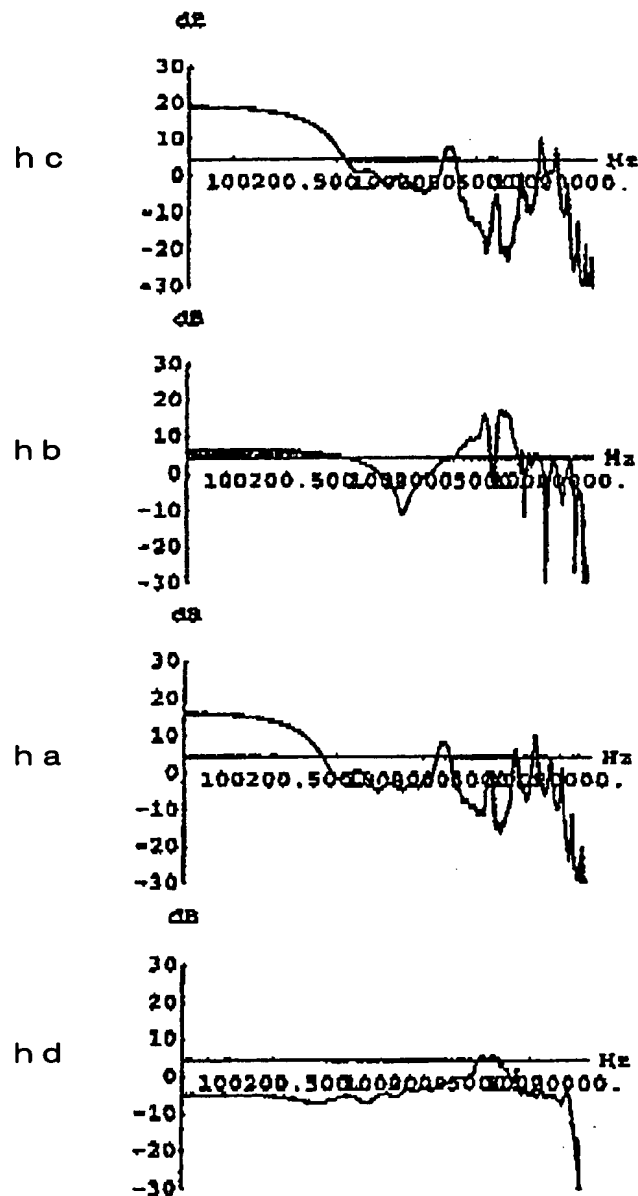
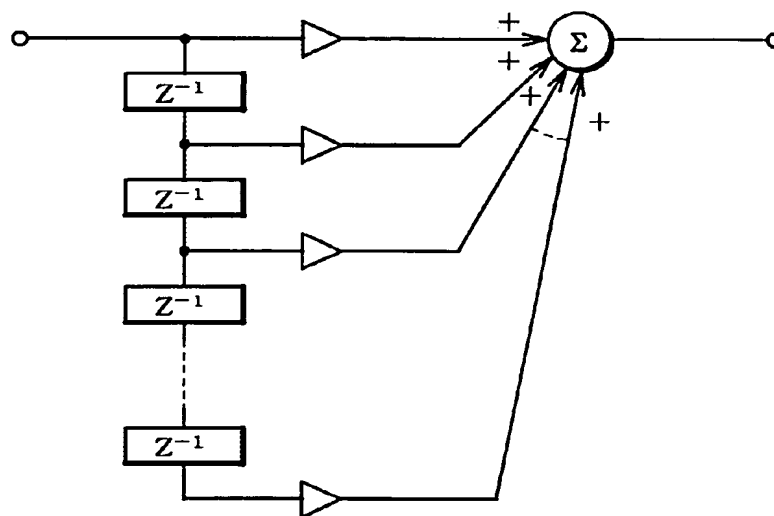


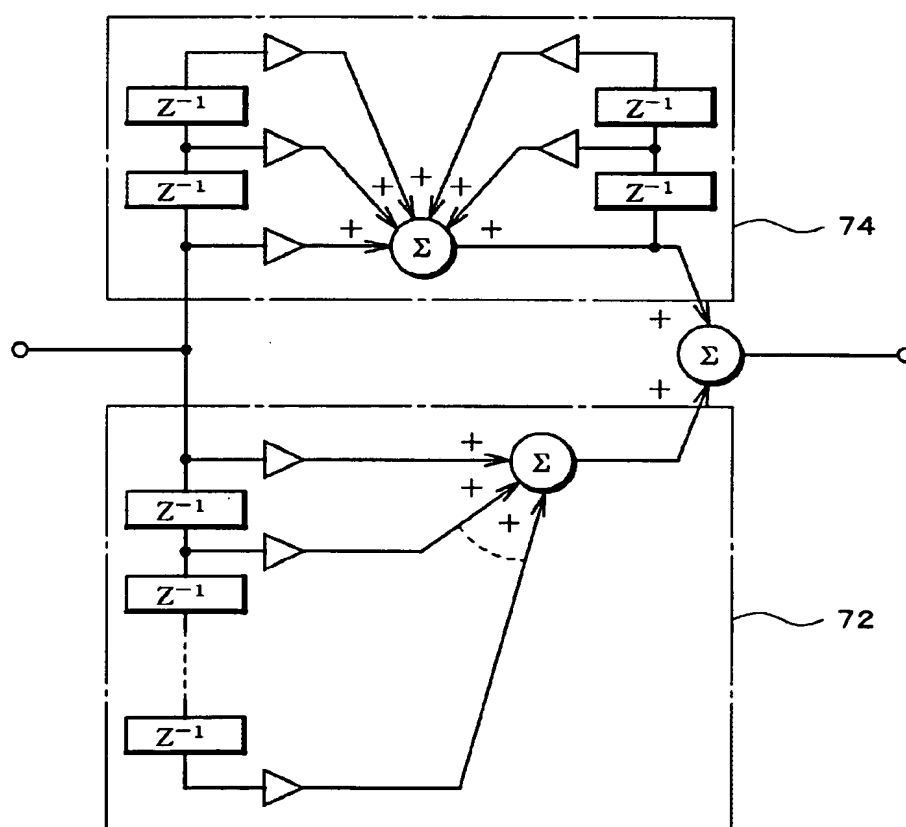
FIG.12



$Z^{-1}$  :DELAY PROCESSING

▷ :COEFFICIENT PROCESSING

FIG.13



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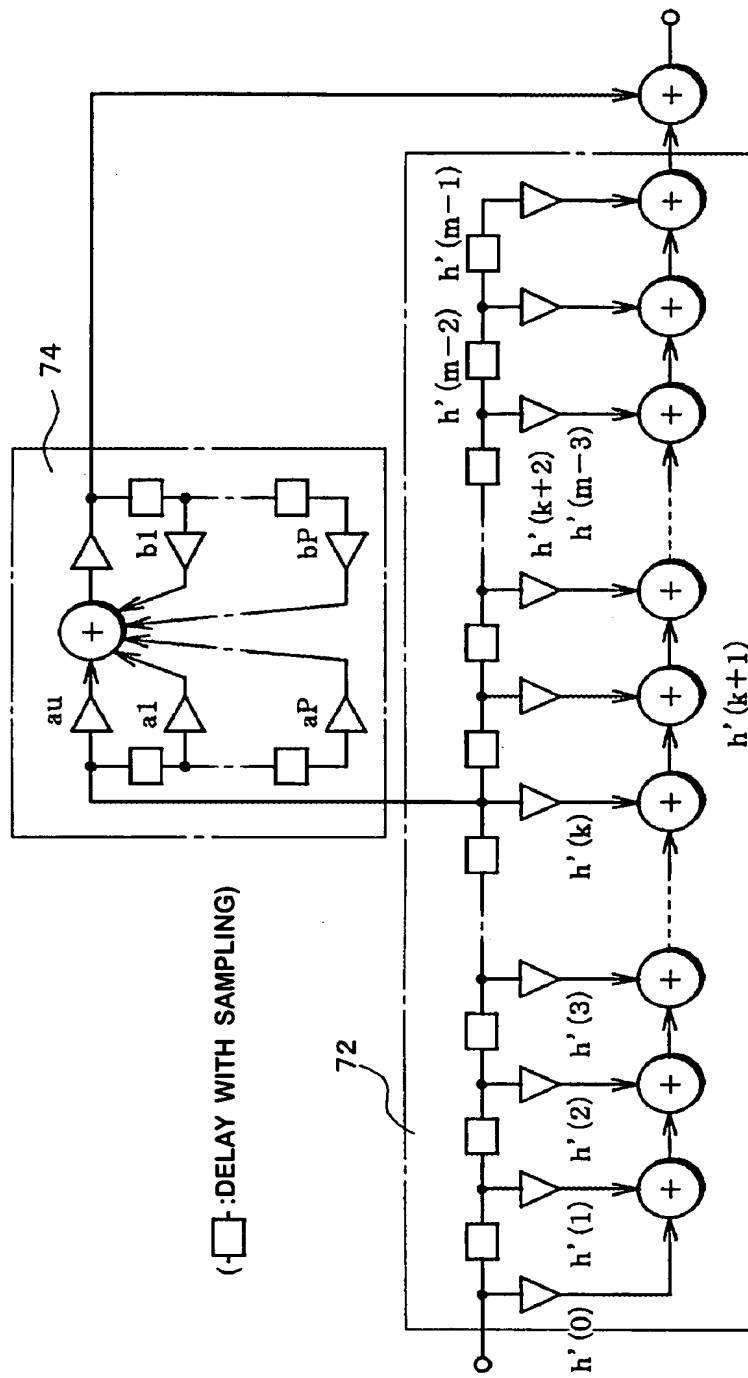


FIG.15

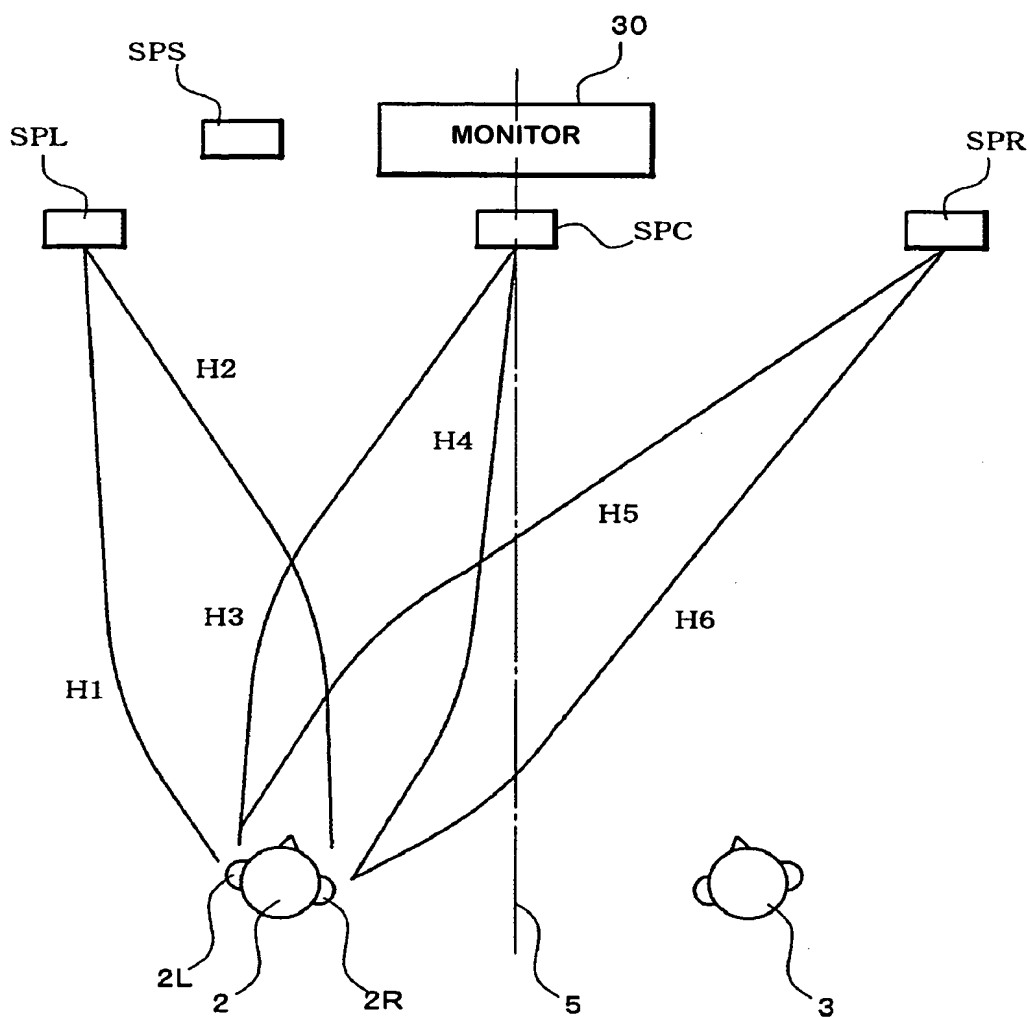


FIG.16

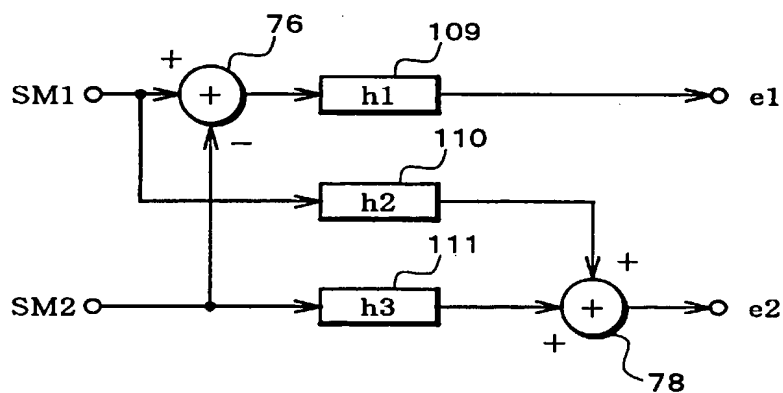
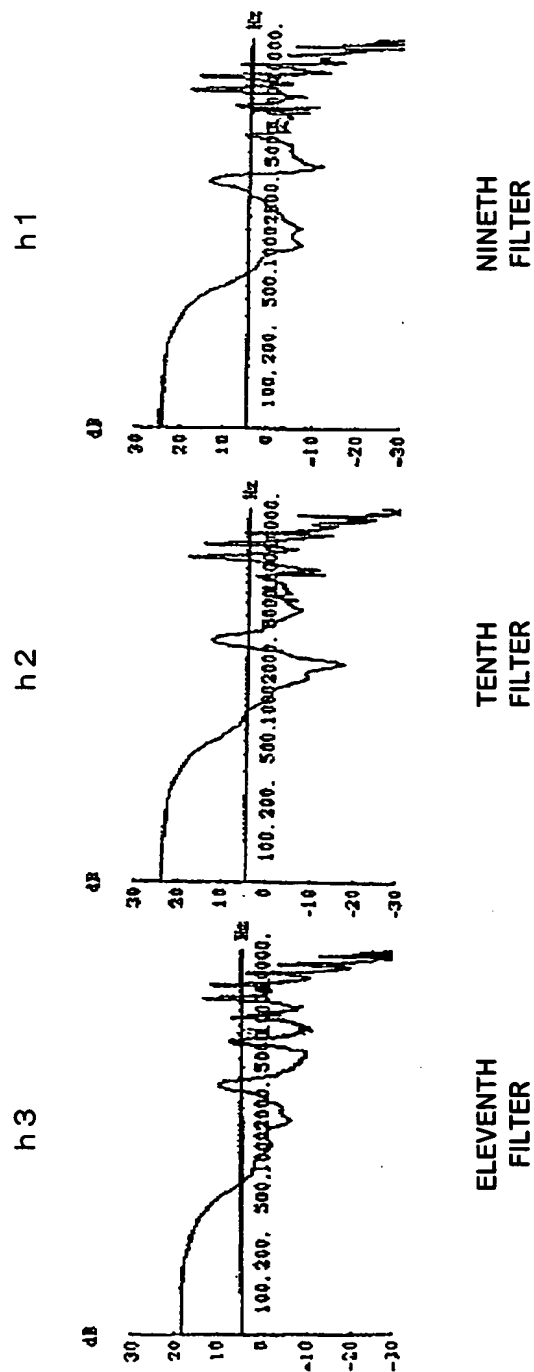
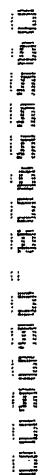




FIG.17



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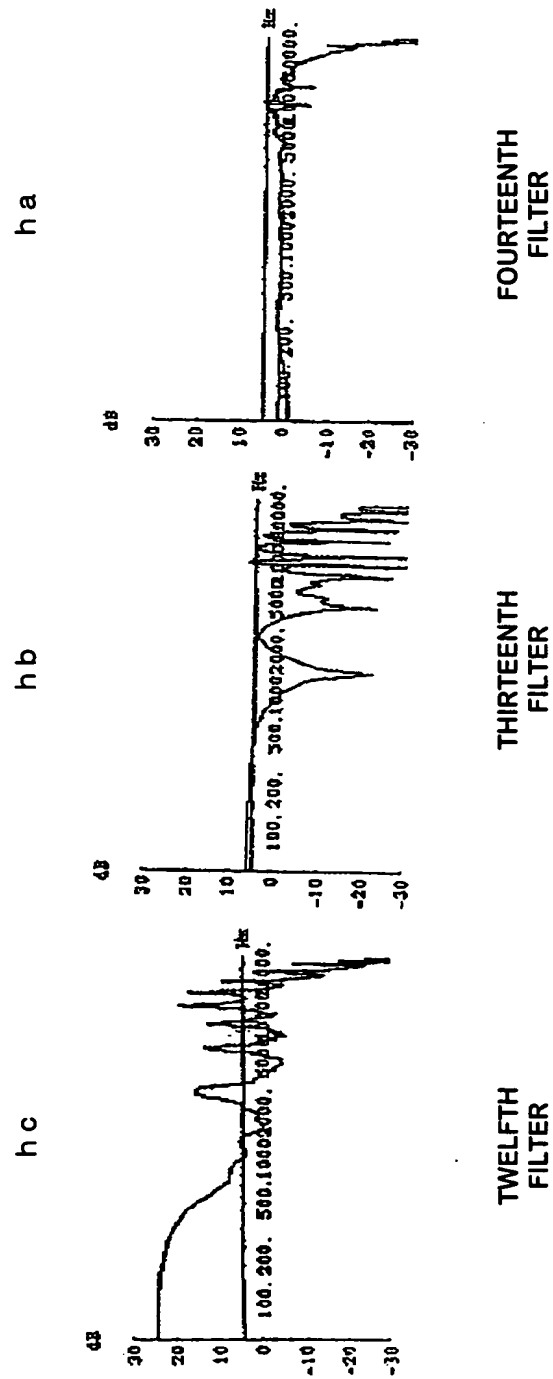


FIG.20

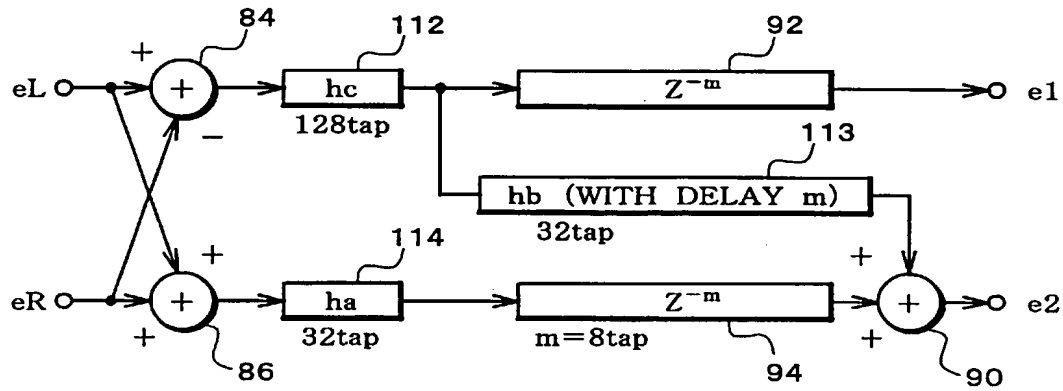
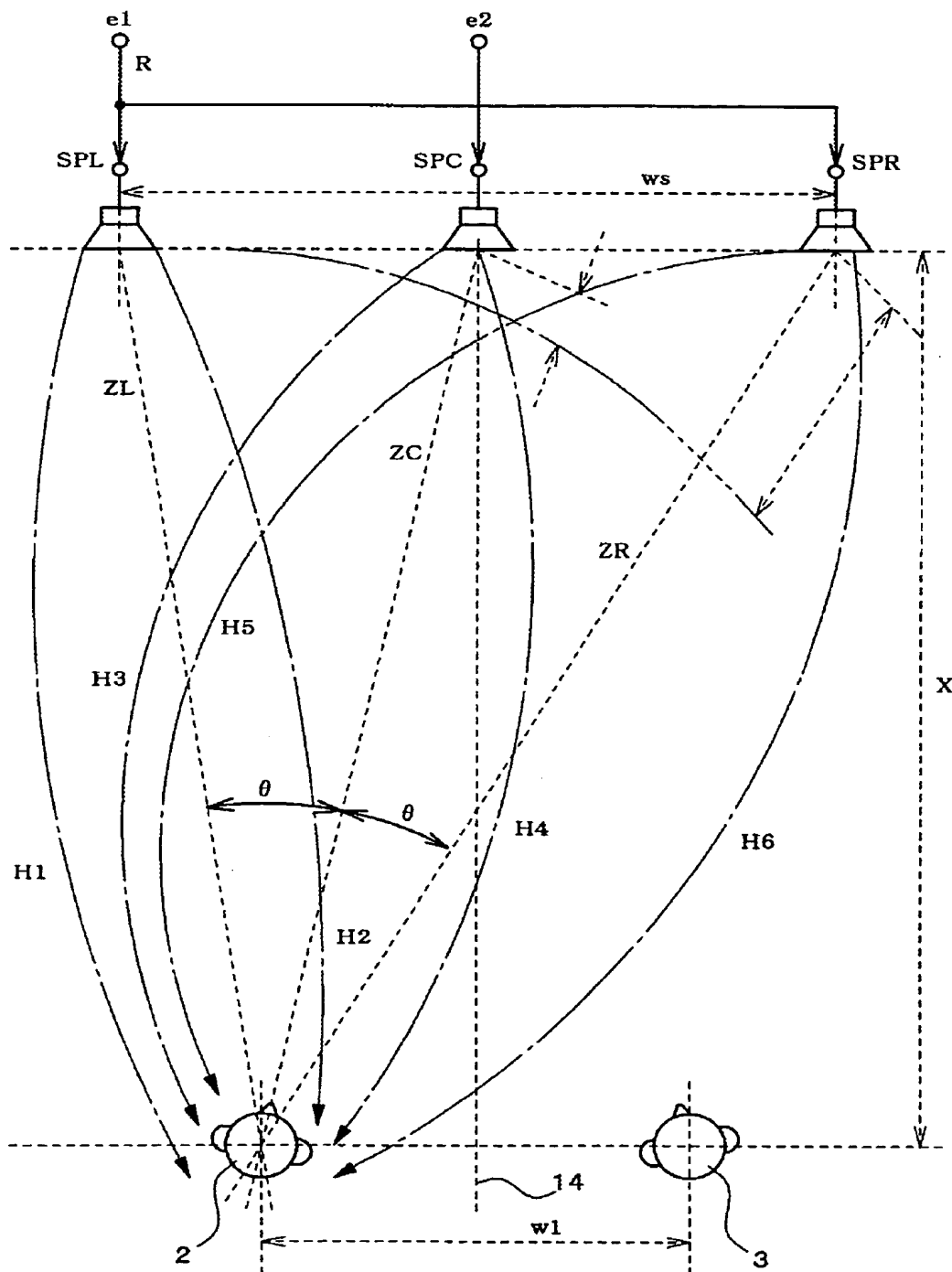


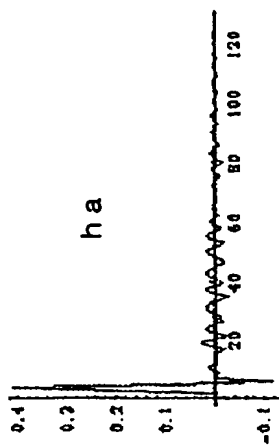
FIG.21



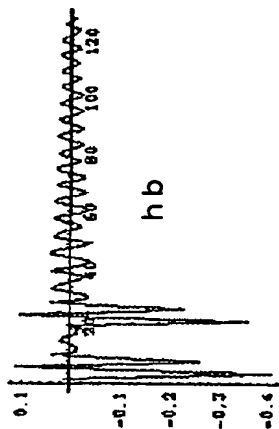
The diagram illustrates a stereo signal processing system. It features two input channels, SML (Stereo Mid Left) and SMR (Stereo Mid Right), each entering a summing junction. The SML channel's summing junction also receives a feedback signal from block 112. The SMR channel's summing junction also receives a feedback signal from block 114. The outputs of these summing junctions are labeled  $e1$  and  $e2$ . These signals pass through gain blocks  $hc'$  (112a) and  $ha'$  (114a) respectively. The outputs of 112a and 114a are then fed into two parallel processing blocks, 112 and 114. Block 112 contains a summing junction (112e) that adds the signal from 112a to a feedback signal from block 96. The output of 112e passes through a delay block  $Z^{-nLR}$  (112c) and a gain block  $\times KLR$  (112d) before being fed back to the SML summing junction. Block 114 contains a similar summing junction (114b) and feedback loop with delay block  $Z^{-nLR}$  (114c) and gain block  $\times KLR$  (114d). The outputs of blocks 112 and 114 are fed into a central processing block 113. Block 113 contains a summing junction (113e) that adds the signals from 112 and 114. The output of 113e passes through a delay block  $Z^{-m}$  (113c) and a gain block  $\times KLR$  (113d) before being fed back to the SMR summing junction. The final output of block 113 is labeled  $e1$ .

FIG.23

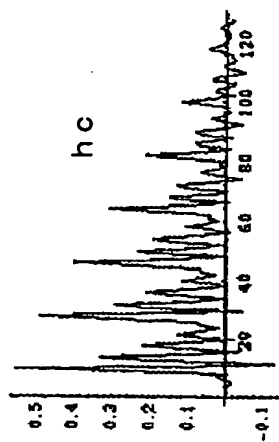
(IN FIG.20)



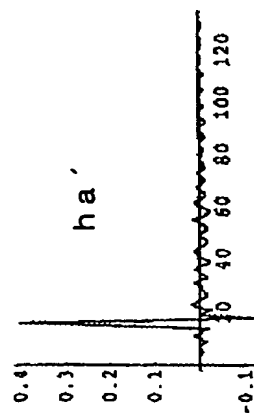
114



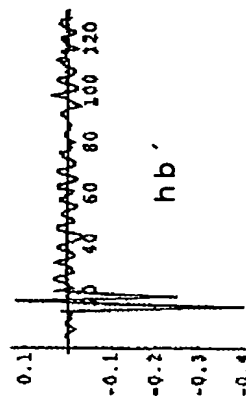
113



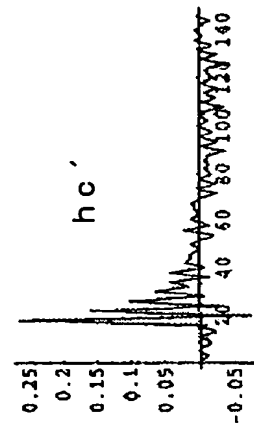
112



114a



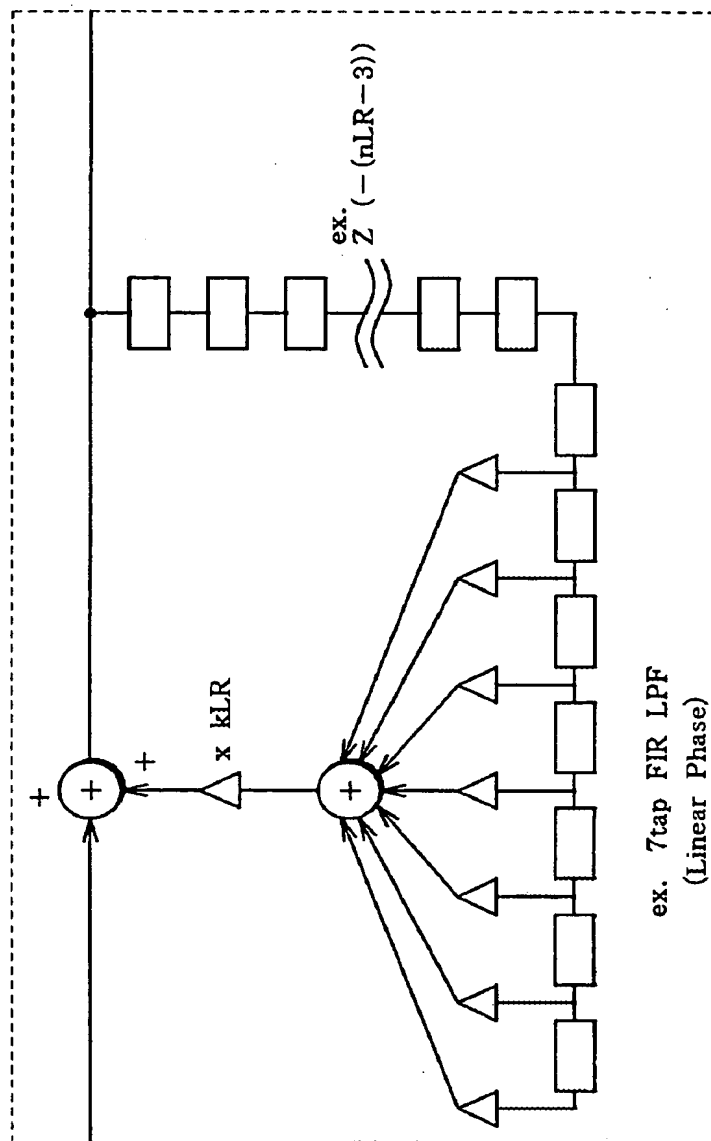
113a



112a

01A 01L 8 (PMT0100) 15

FIG.24



□ : DELAY PROCESSING

△ : COEFFICIENT PROCESSING



FIG.25A



FIG.25B

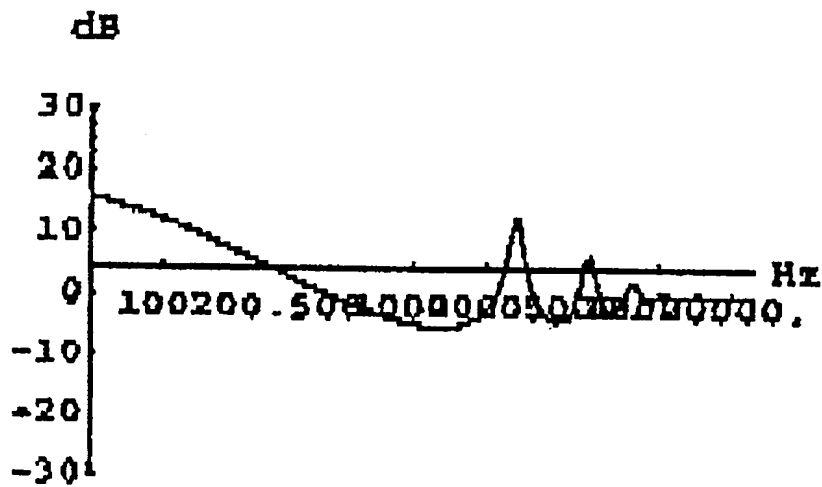
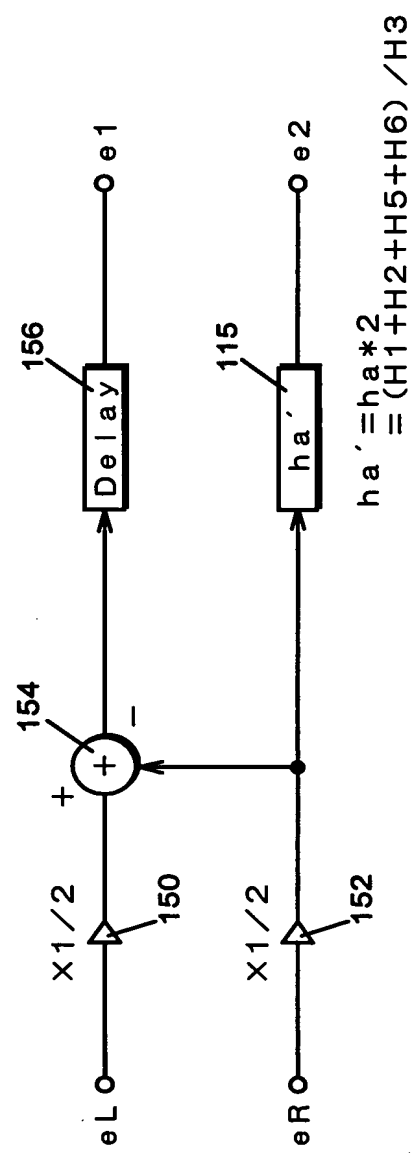


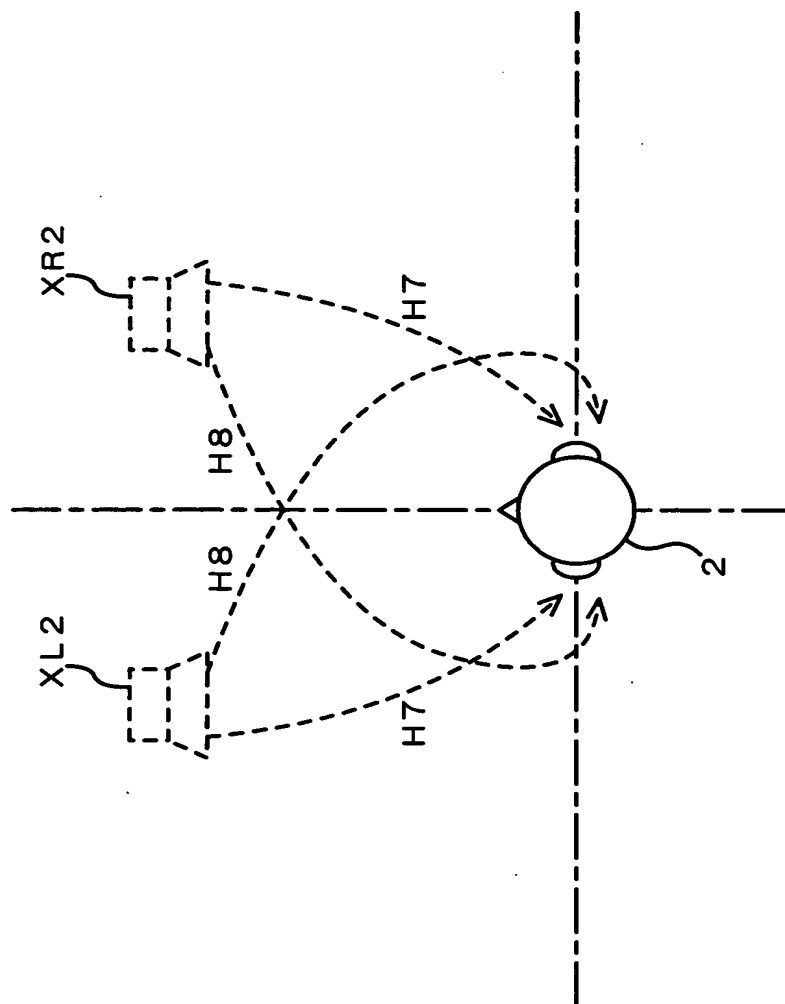
FIG.26



005050-806550

005050-806550

FIG.27



The diagram illustrates a stereo signal processing system with feedback loops. It features three input signals: FCO, FLO, and FRO. FLO and FRO are processed by a series of adders (160, 166, 162) and delay blocks (164L, 164C, 164R) to produce Lout, Cout, and Rout. A feedback loop involving a high-pass filter (HPF 32) and adder 168 is also shown. The system includes two parallel processing paths (12 and 34) containing adaptive filters (APF1 36, APF2 38), delay blocks (h1 101, h2 102, h3 103, h4 104), and adders (44, 45). Error signals e1 and e2 are used for feedback.

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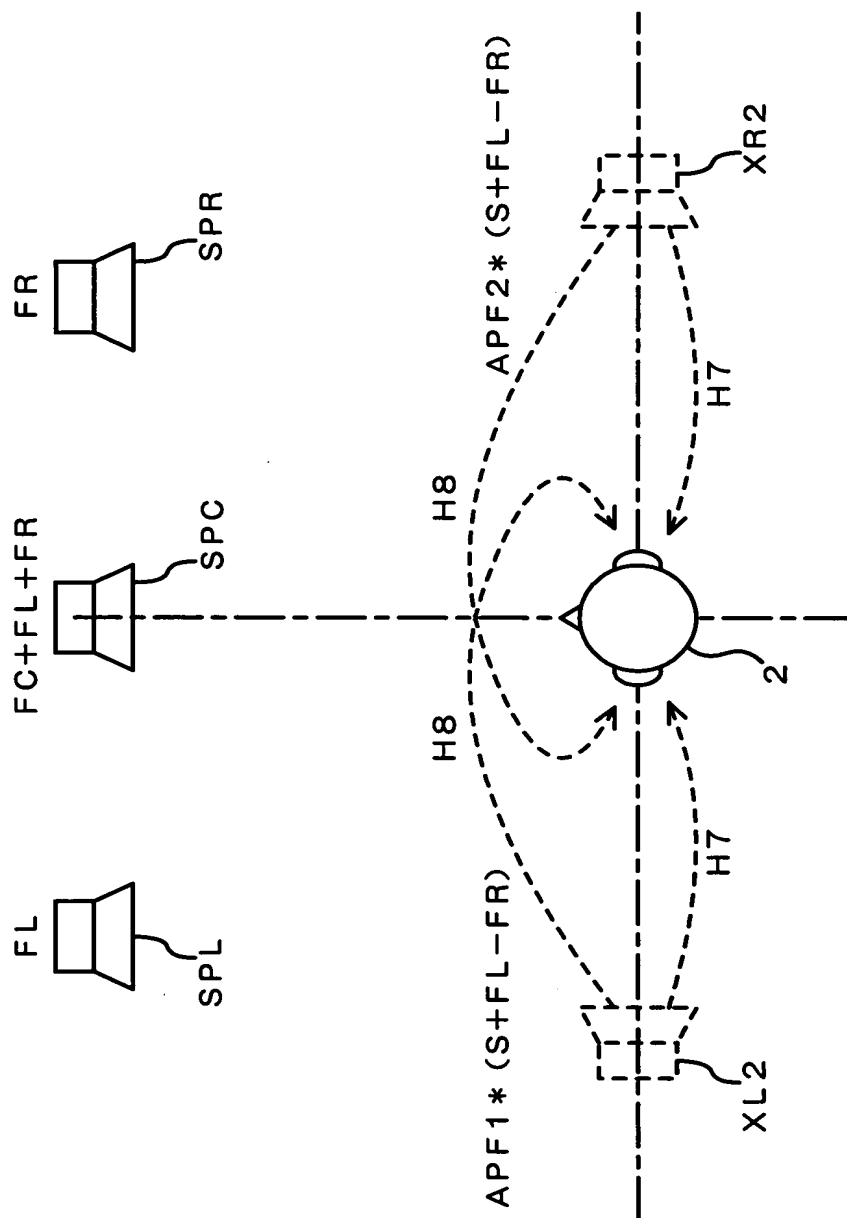


FIG.30

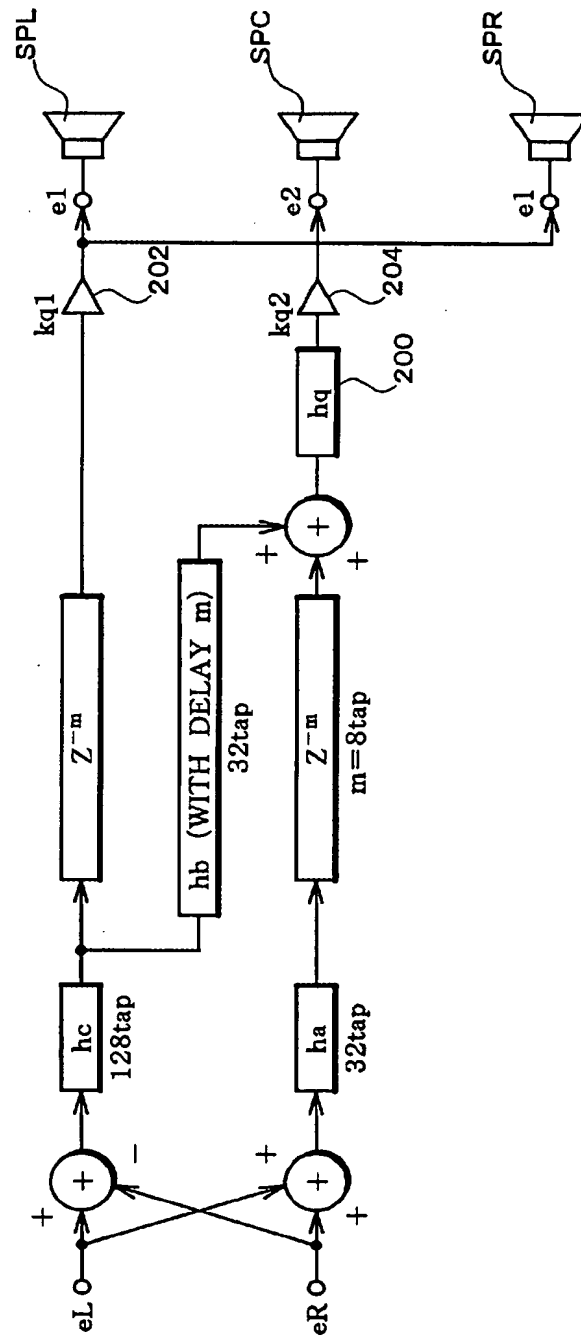


FIG.31

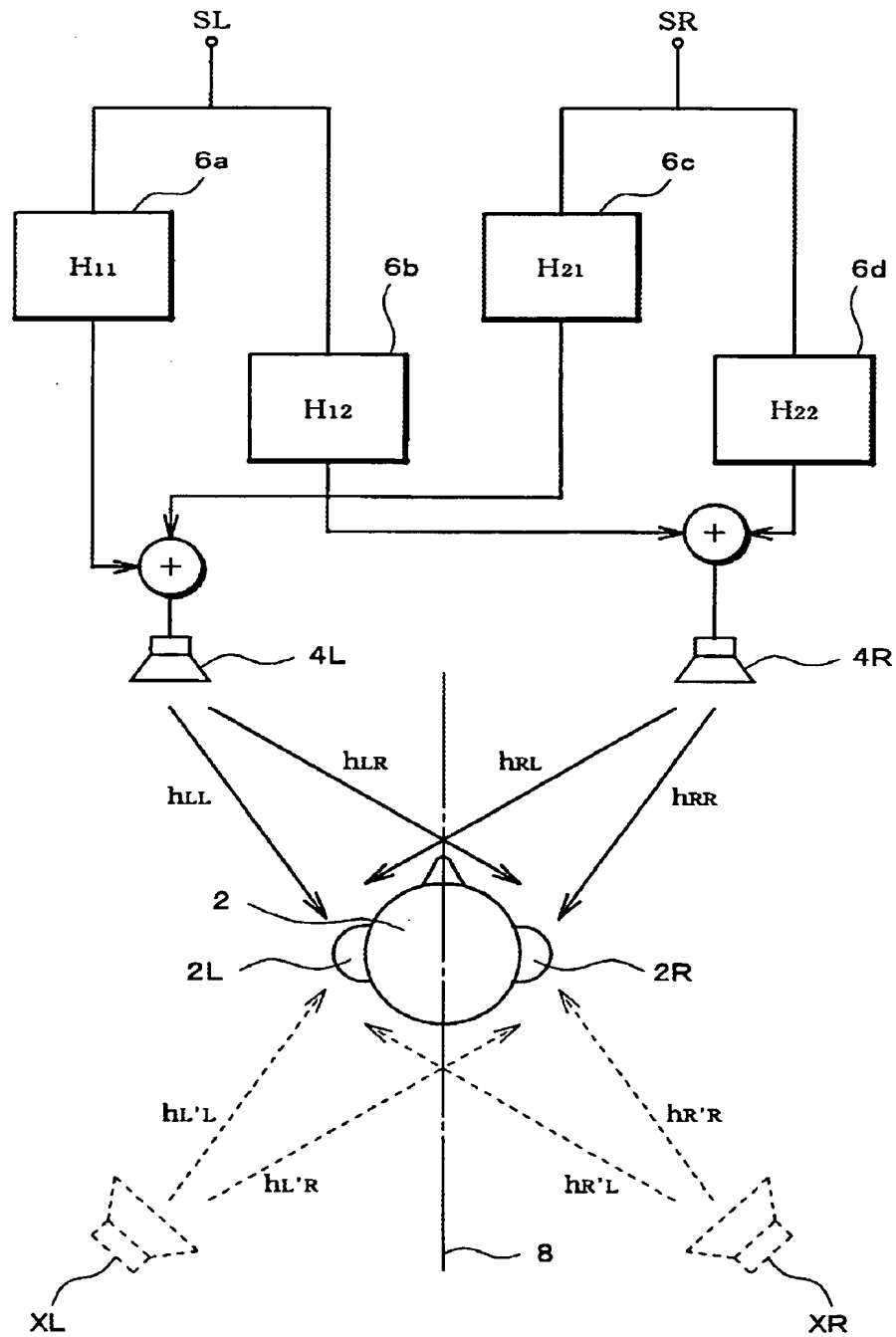


FIG.32

